Inventor: Iwanishi, et al
Docket No.: 10873.1199US01
Title: METHOD FOR DESIGNING SEMICONDUCTOR INTEGRATED CIRCUIT
Attorney Name: Douglas P. Mueller
Phone No.: (612) 371-5237
Sheet 1 of 23

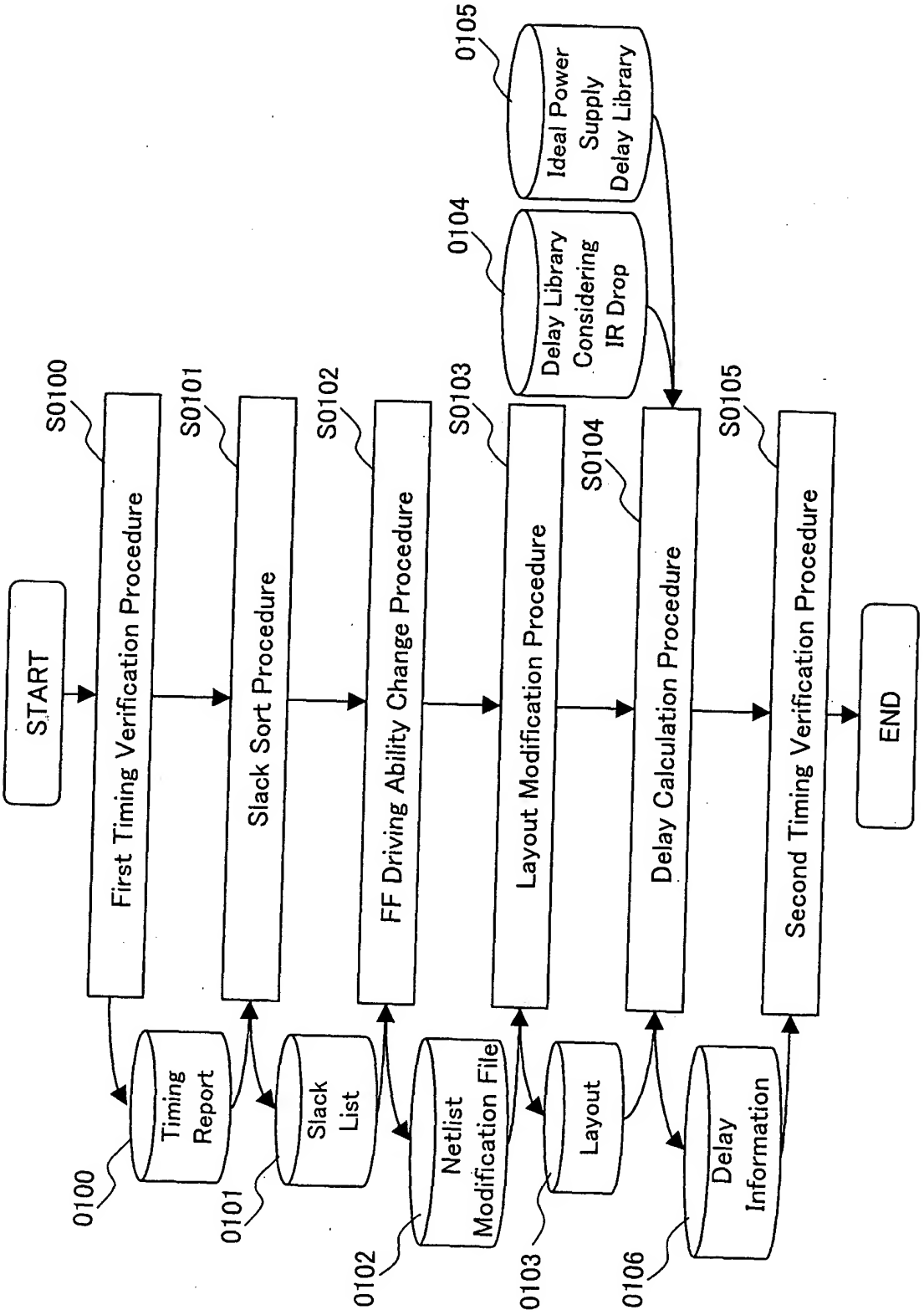

FIG. 1

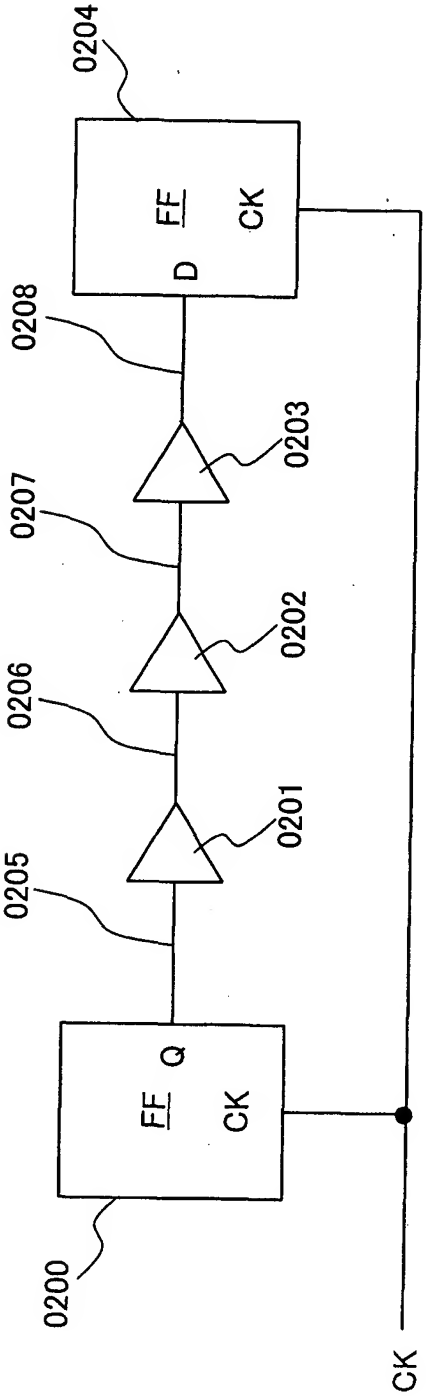

FIG. 2A

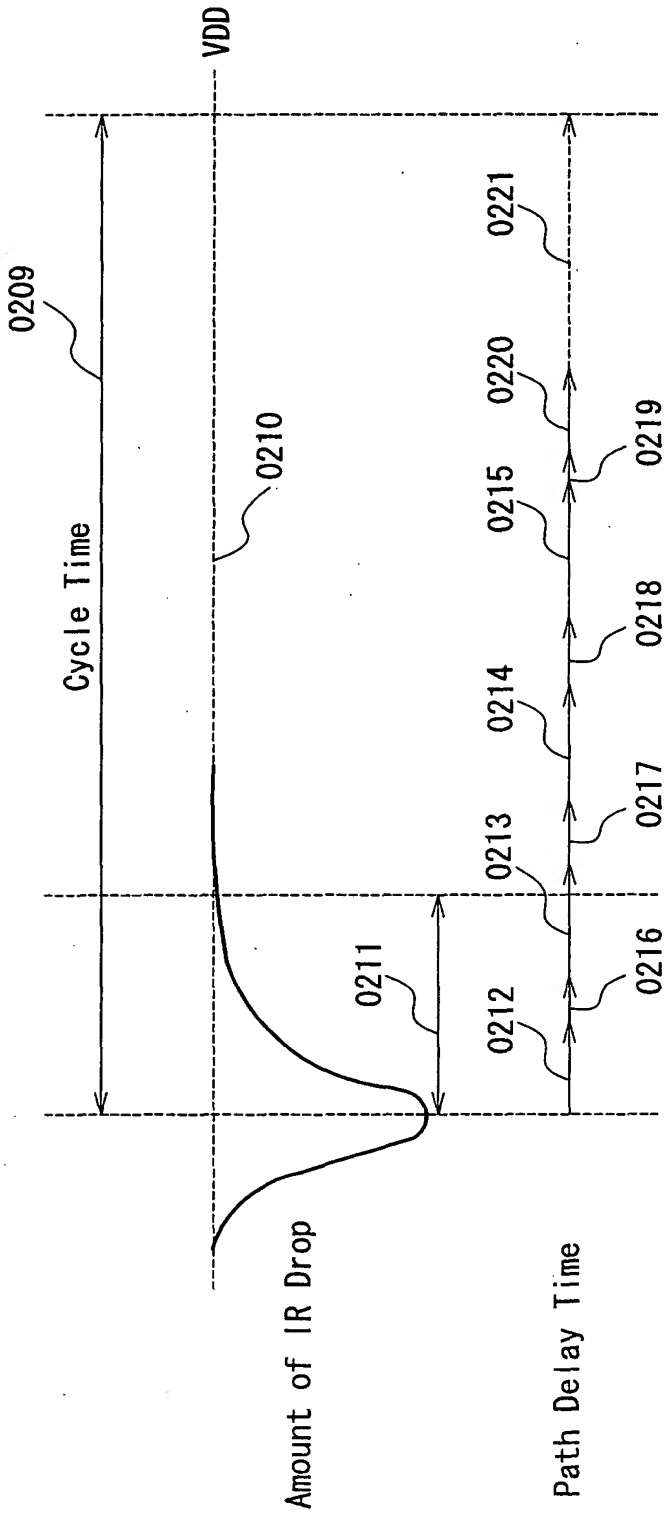
VDD
0209
Cycle Time
0210
0211
0212
0213
0214
0215
0216
0217
0218
0219
0220
0221
Amount of IR Drop
Path Delay Time

FIG. 2B

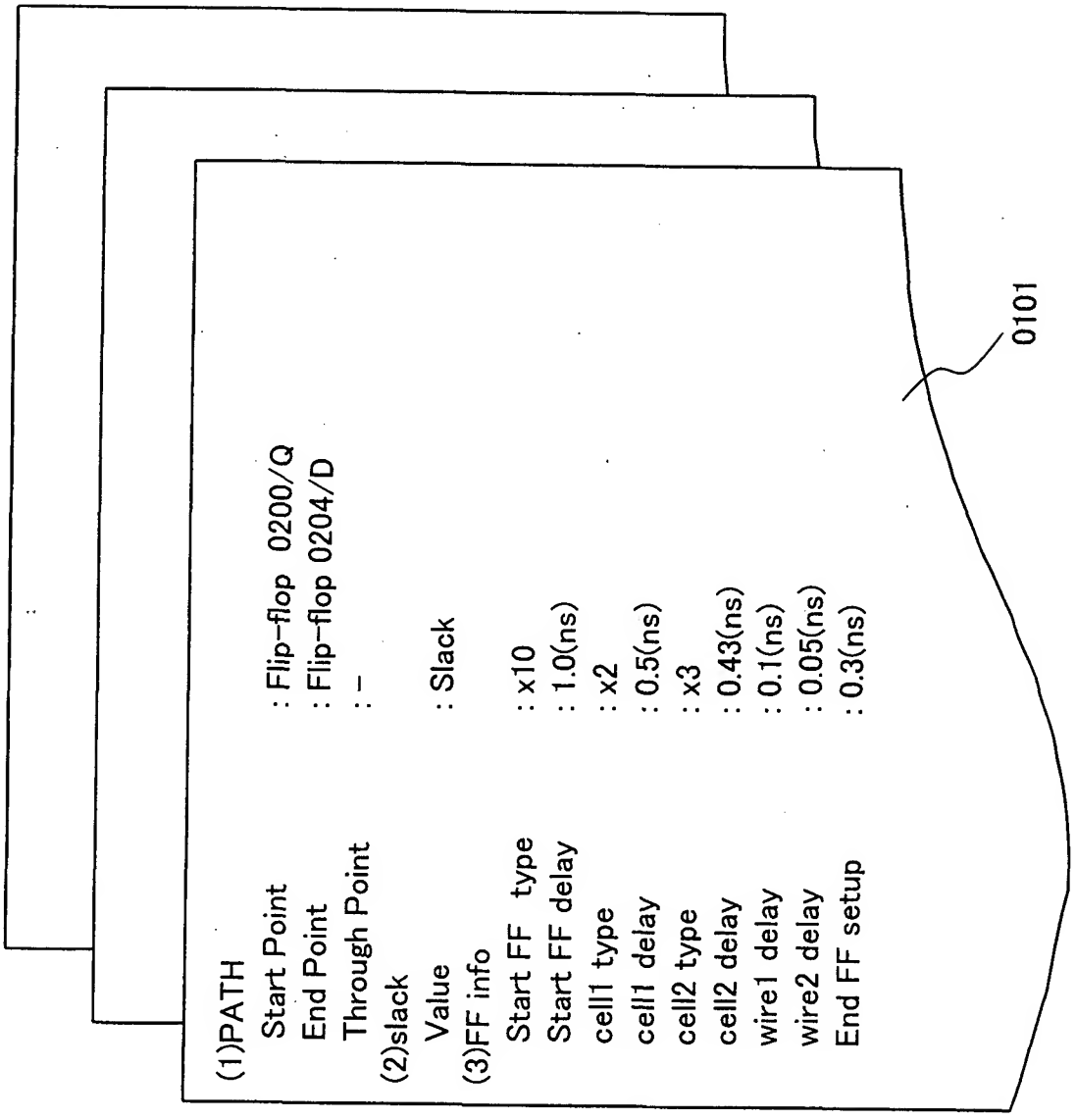
(1)PATH
Start Point : Flip-flop 0200/Q
End Point : Flip-flop 0204/D
Through Point : -
(2)slack
Value : Slack
(3)FF info
Start FF type : x10
Start FF delay : 1.0(ns)
cell1 type : x2
cell1 delay : 0.5(ns)
cell2 type : x3
cell2 delay : 0.43(ns)
wire1 delay : 0.1(ns)
wire2 delay : 0.05(ns)
End FF setup : 0.3(ns)
0101

FIG. 3

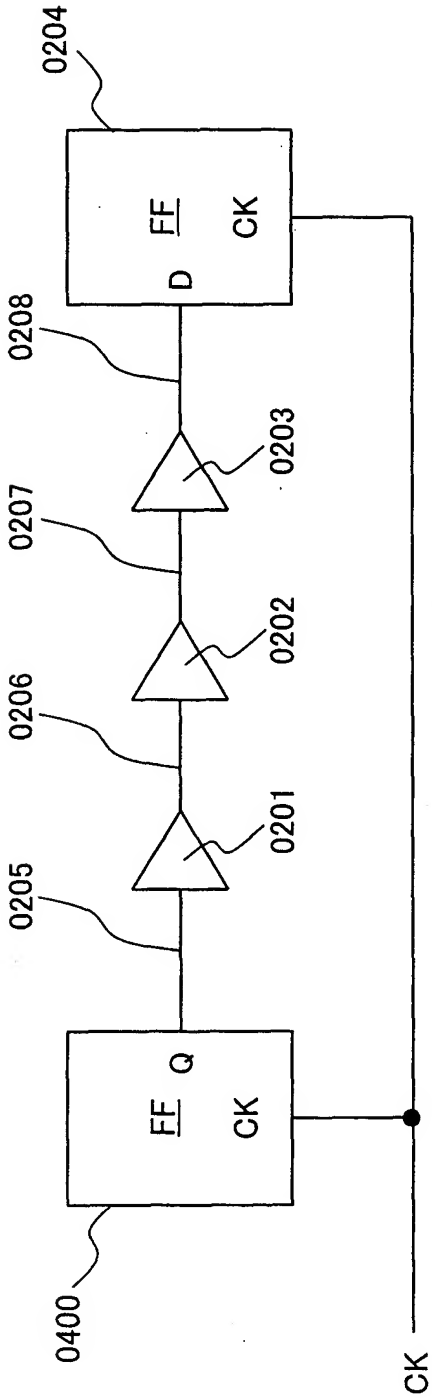

FIG. 4A

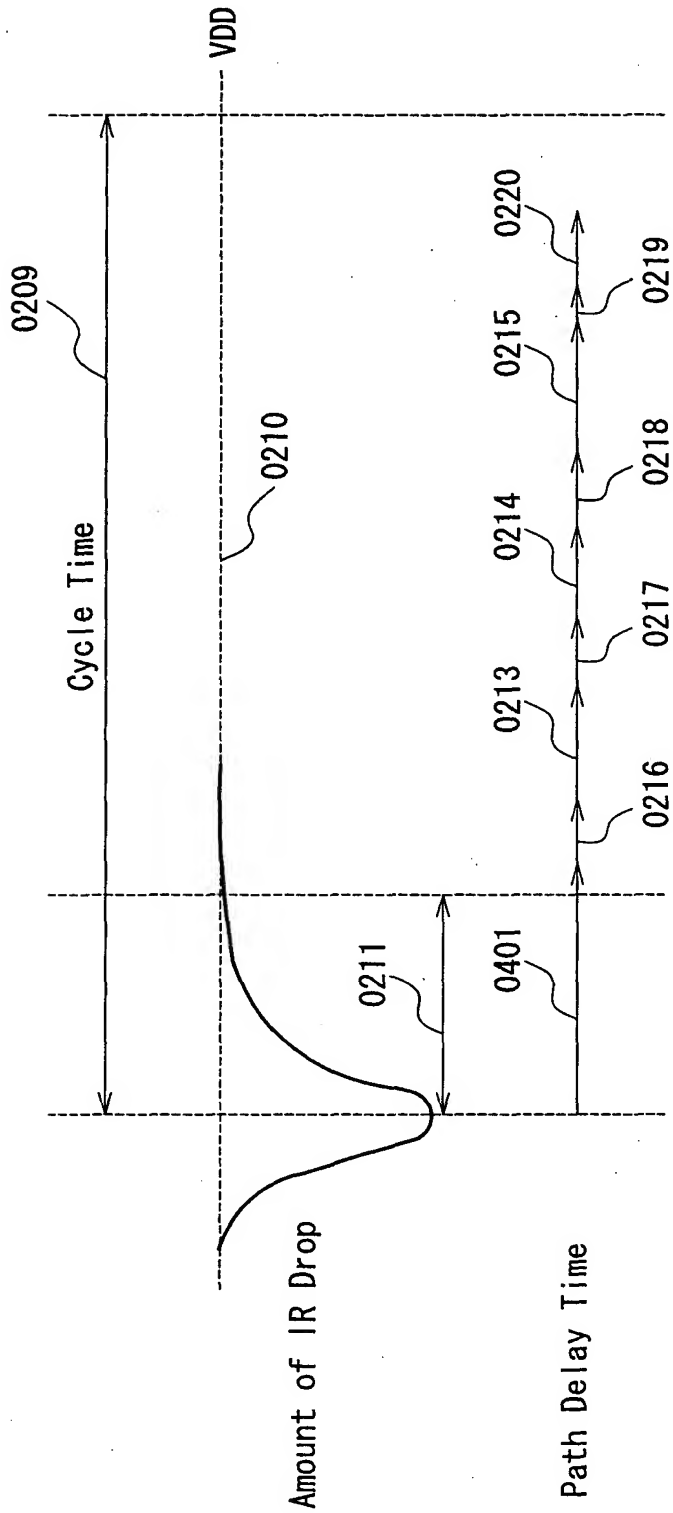
VDD
0209
Cycle Time
0210
0211
0401
0213
0214
0215
0216
0217
0218
0219
0220
Amount of IR Drop
Path Delay Time

FIG. 4B

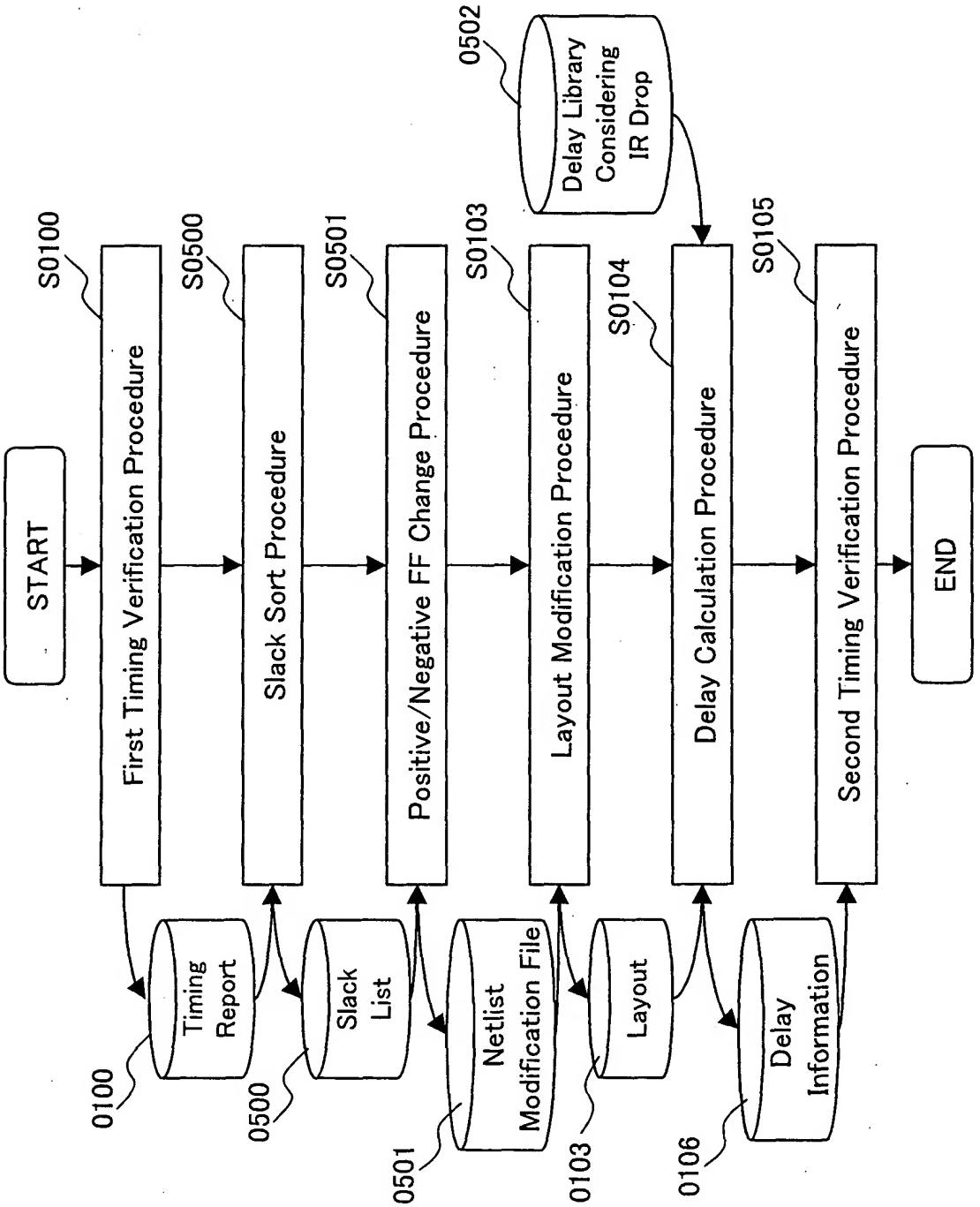
START
S0100
First Timing Verification Procedure
S0500
Slack Sort Procedure
S0501
Positive/Negative FF Change Procedure
S0103
Layout Modification Procedure
S0104
Delay Calculation Procedure
S0105
Second Timing Verification Procedure
END
0502
Delay Library Considering IR Drop
Timing Report
0100
Slack List
0500
Netlist Modification File
0501
Layout
0103
Delay Information
0106

FIG. 5

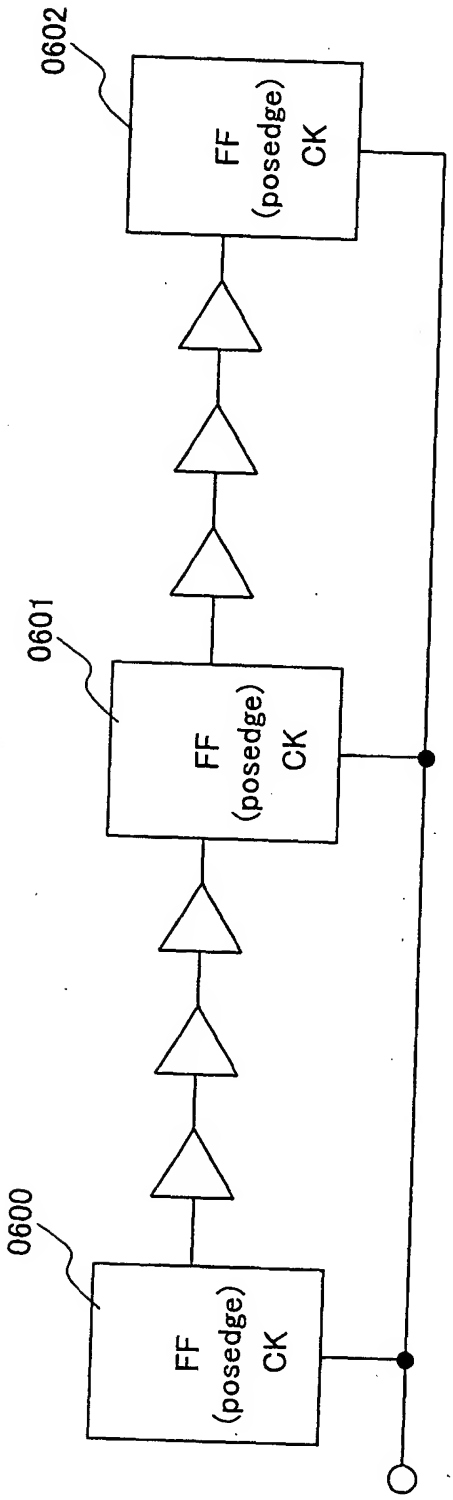

FIG. 6A

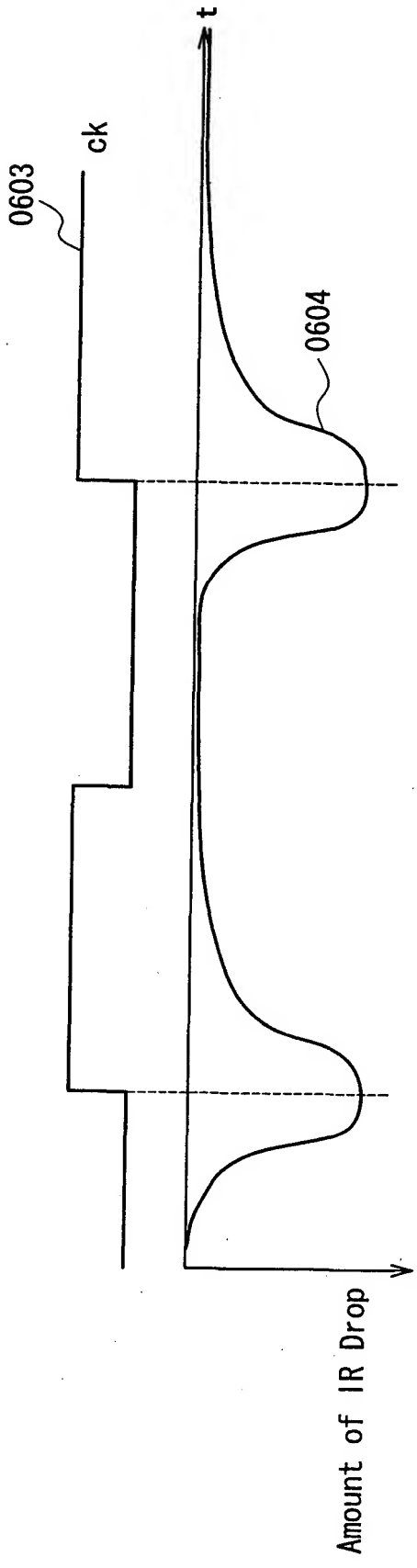

FIG. 6B

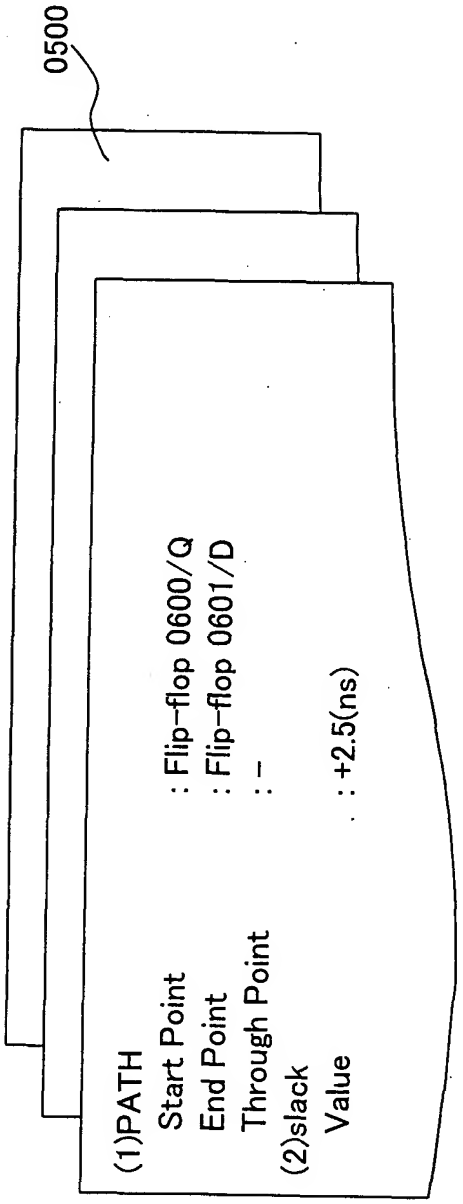
0500
(1)PATH
Start Point : Flip-flop 0600/Q
End Point : Flip-flop 0601/D
Through Point : -
(2)slack
Value : +2.5(ns)

FIG. 6C

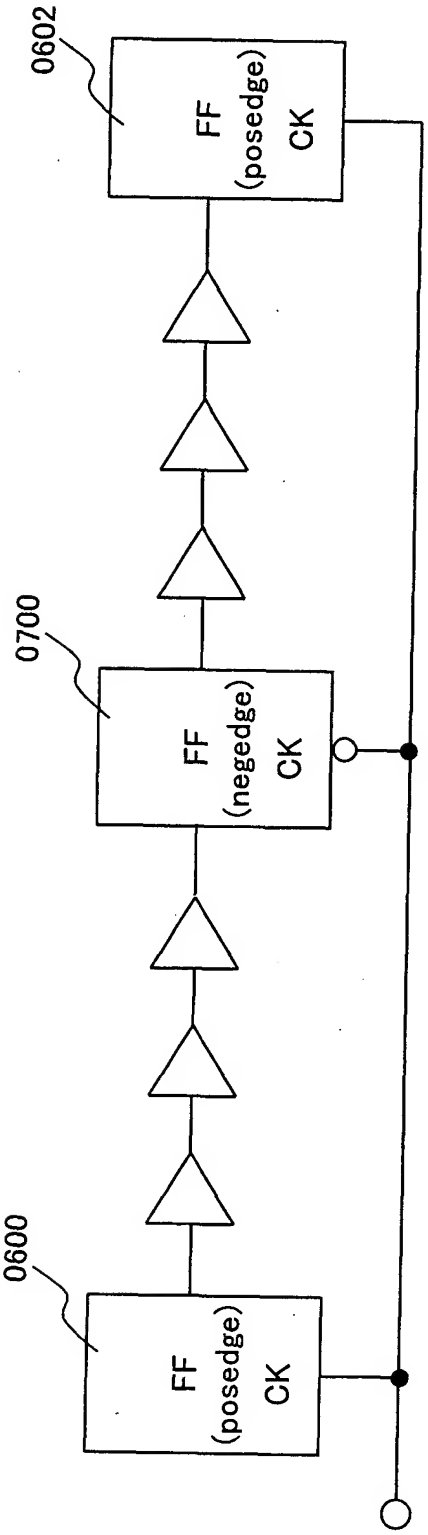

FIG. 7A

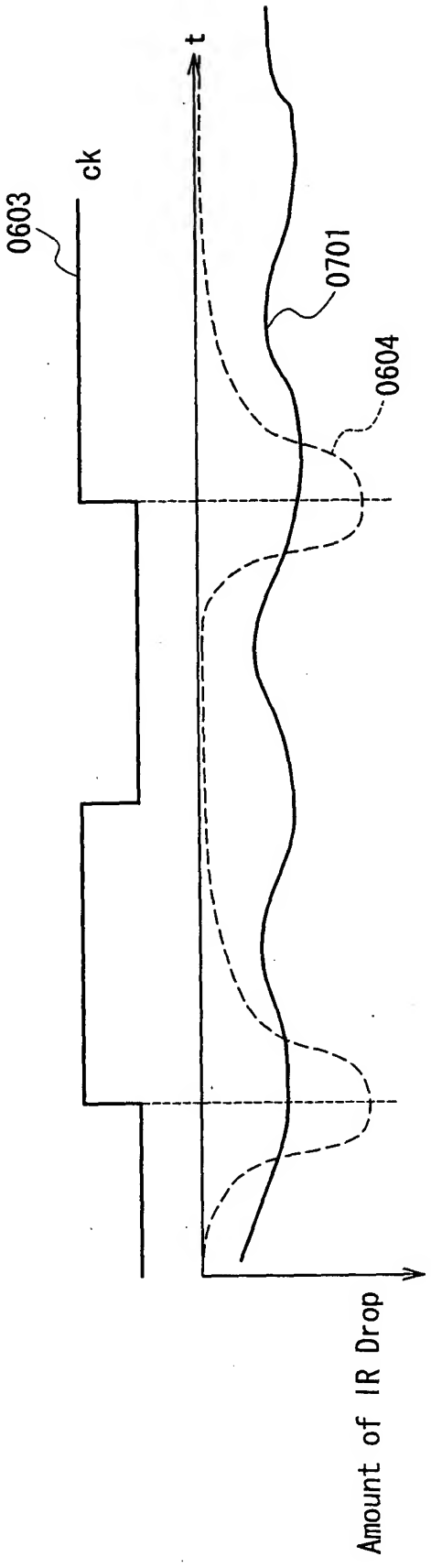

FIG. 7B

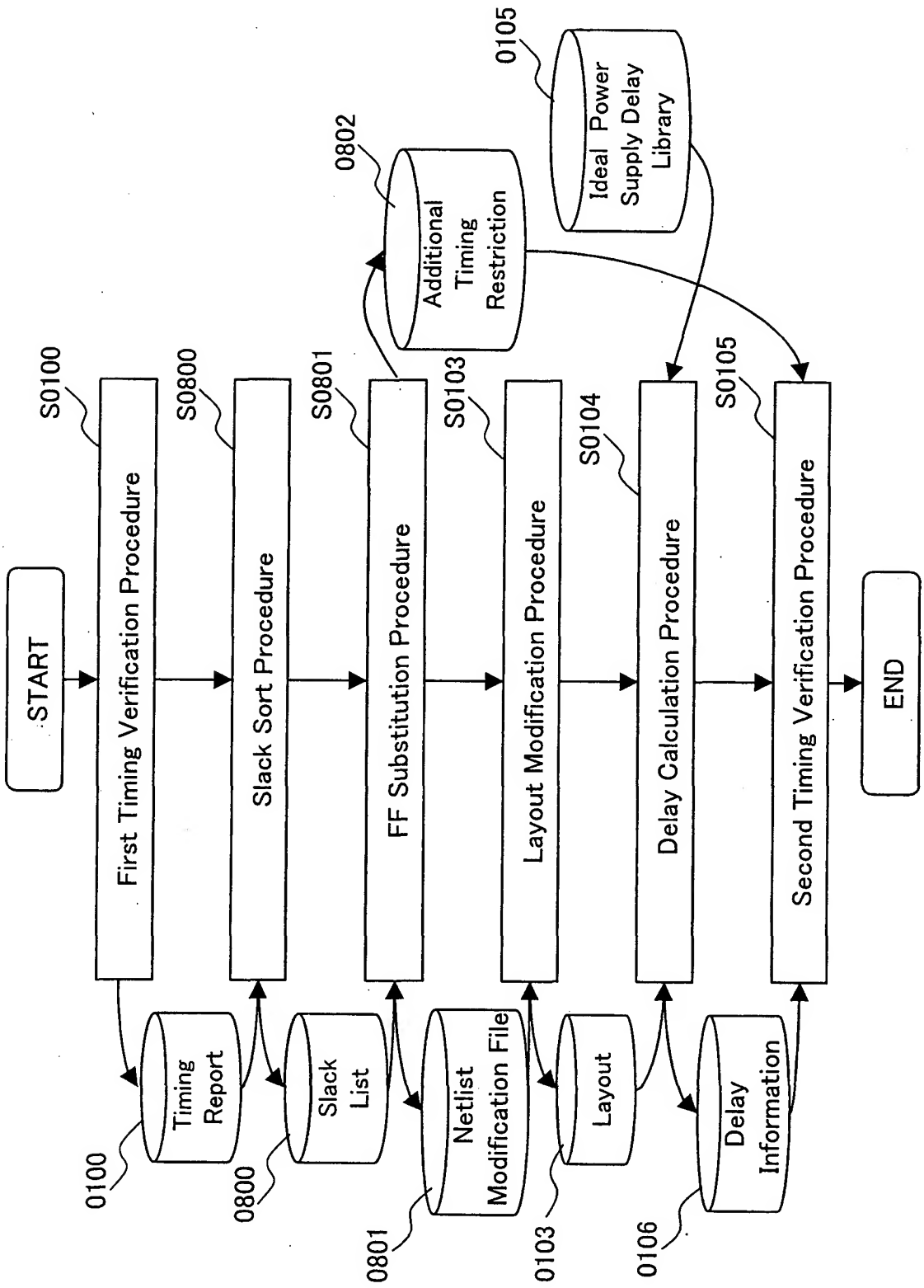
START
S0100
First Timing Verification Procedure
S0800
Slack Sort Procedure
S0801
FF Substitution Procedure
S0103
Layout Modification Procedure
S0104
Delay Calculation Procedure
S0105
Second Timing Verification Procedure
END
0802
Additional Timing Restriction
0105
Ideal Power Supply Delay Library
Timing Report
0100
Slack List
0800
Netlist Modification File
0801
Layout
0103
Delay Information
0106

FIG. 8

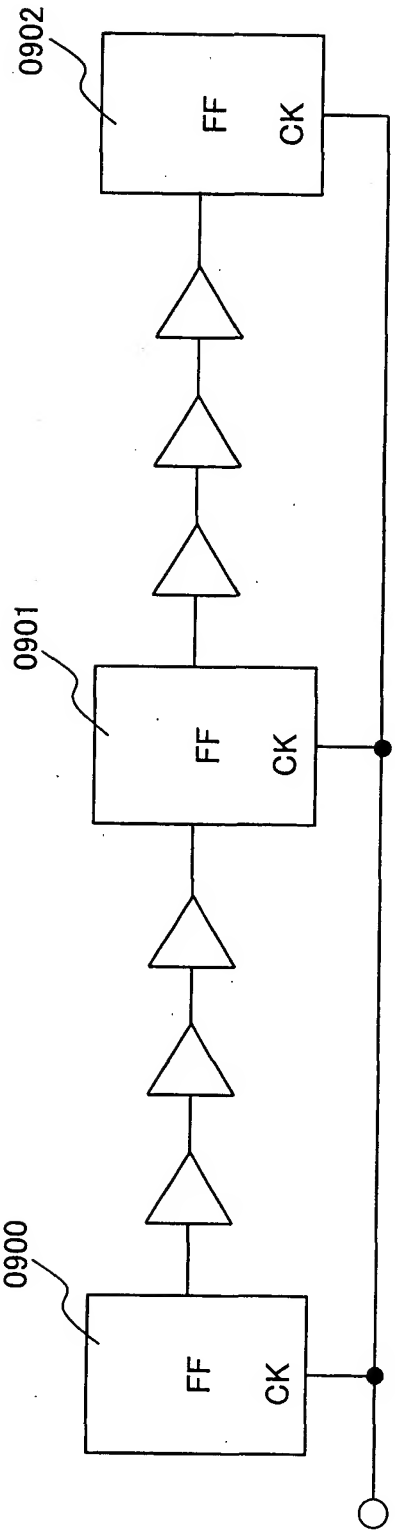

FIG. 9A

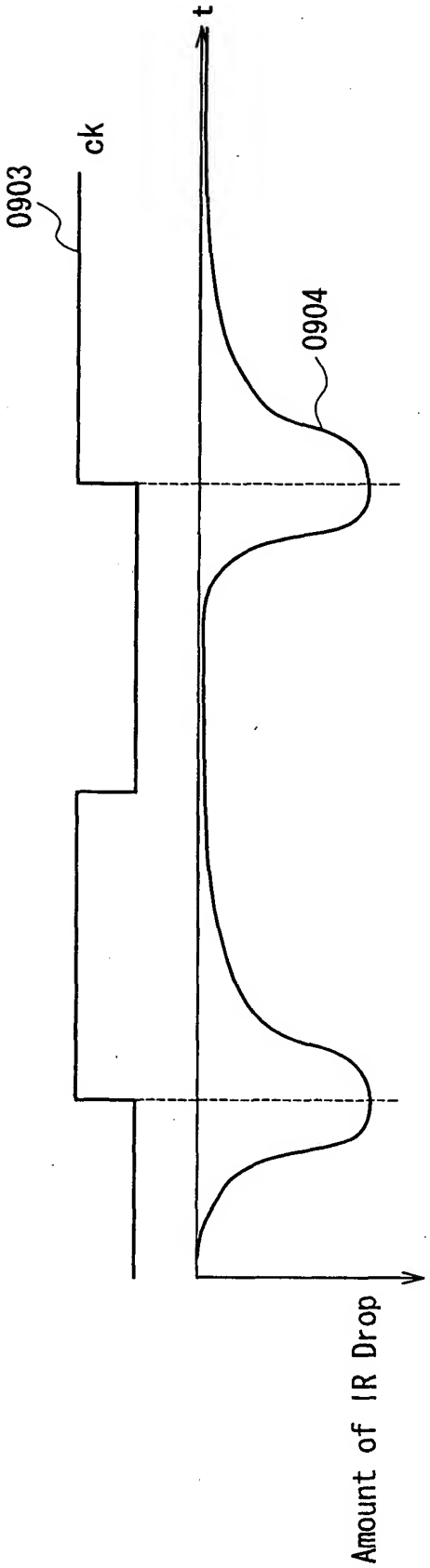

FIG. 9B

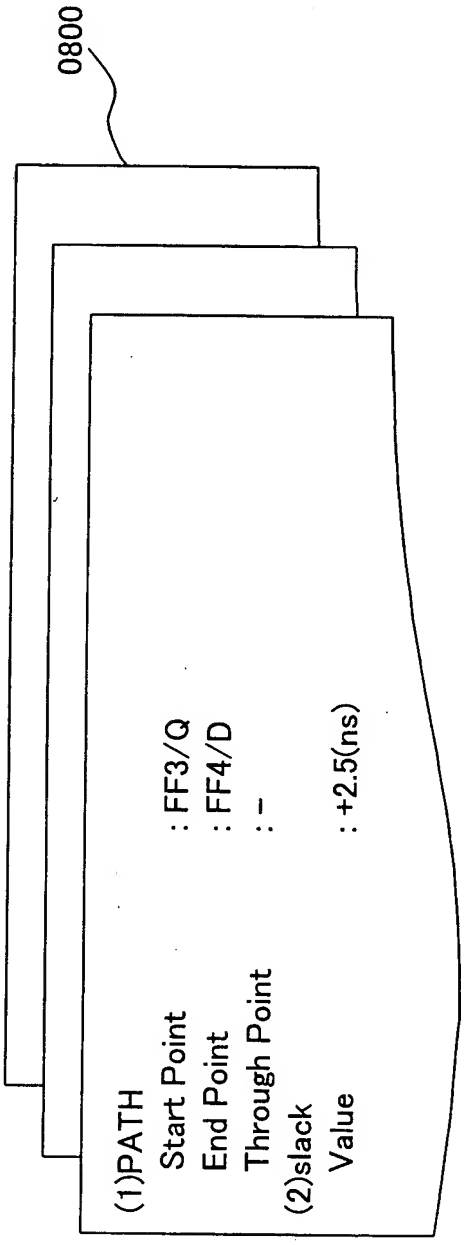
0800
(1)PATH
Start Point : FF3/Q
End Point : FF4/D
Through Point : -
(2)slack
Value : +2.5(ns)

FIG. 9C

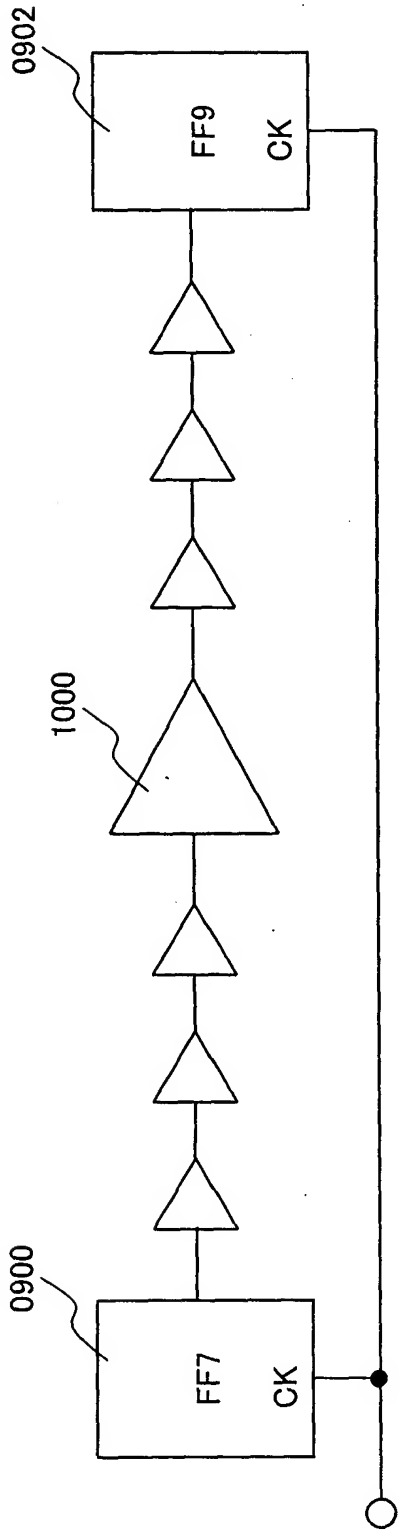

FIG. 10A

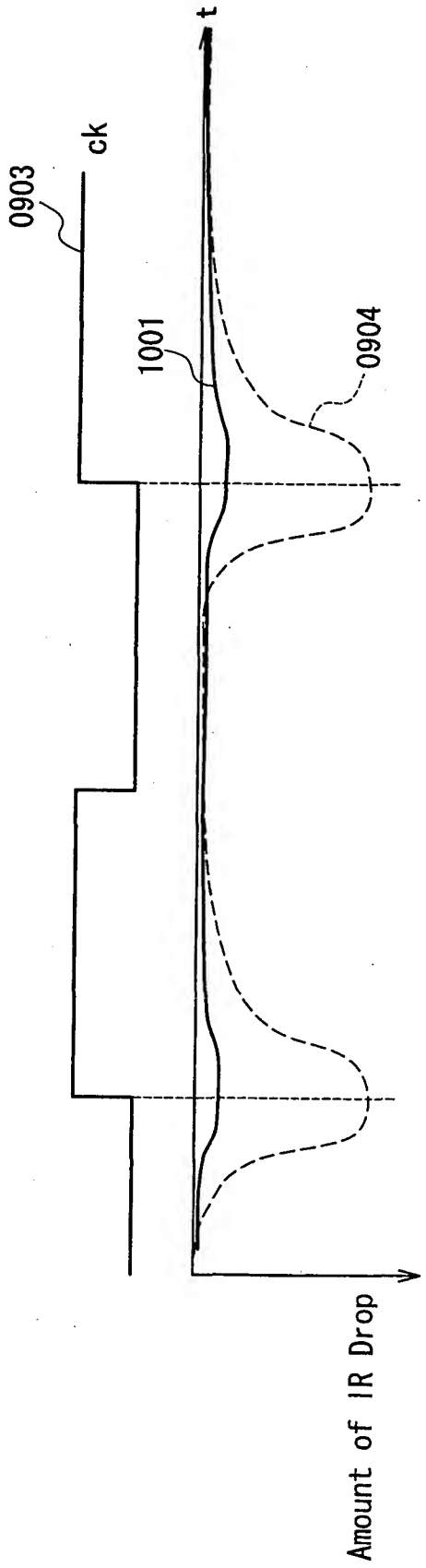

FIG. 10B

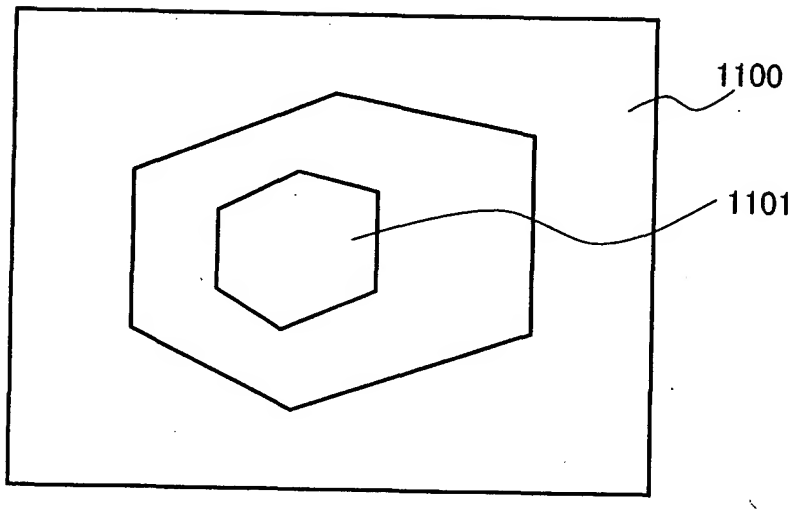

FIG. 11A
PRIOR ART

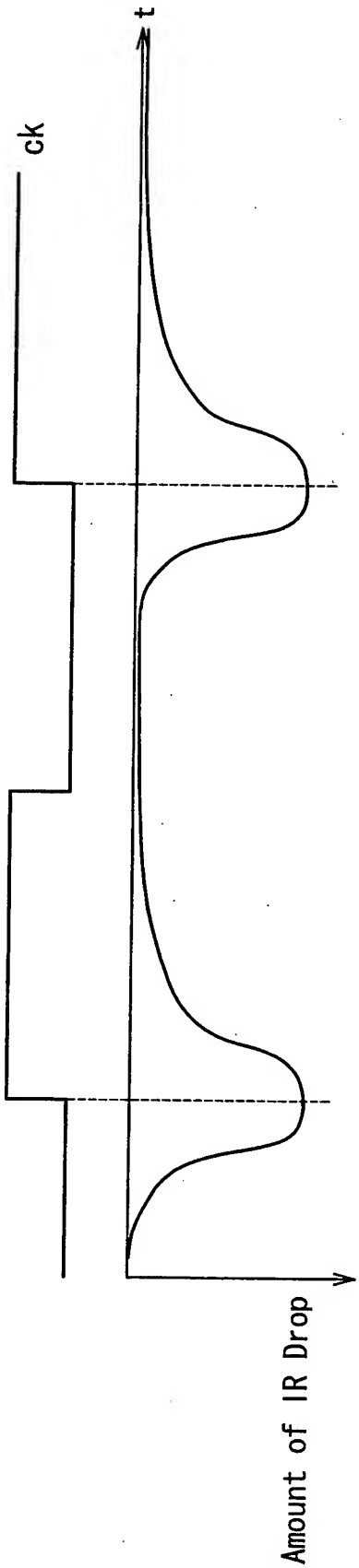

FIG. 11B
PRIOR ART

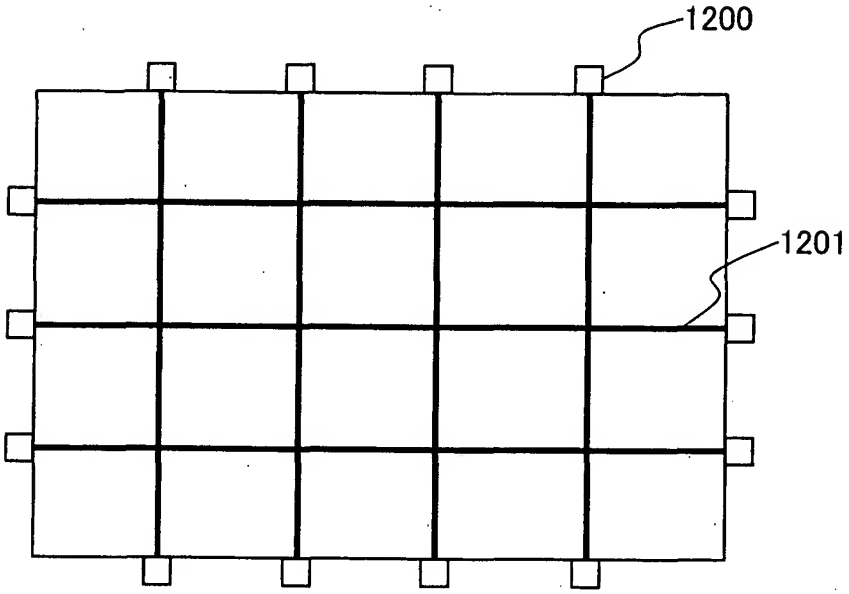

FIG. 12A
PRIOR ART

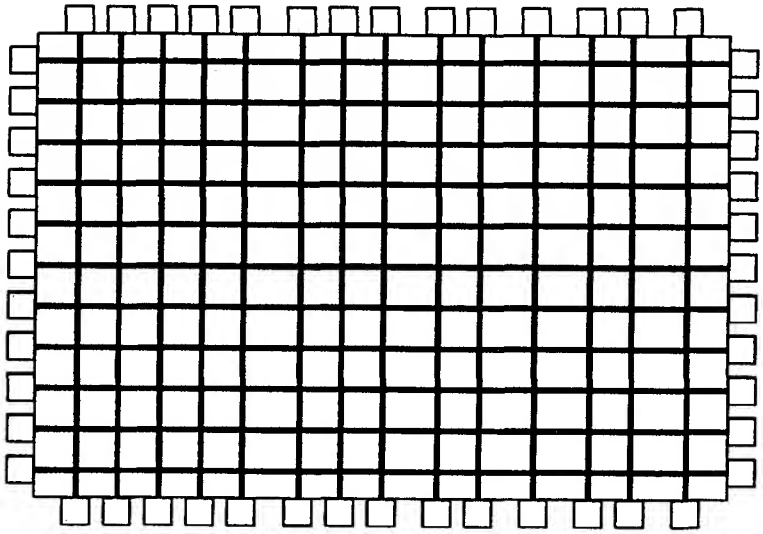

FIG. 12B
PRIOR ART

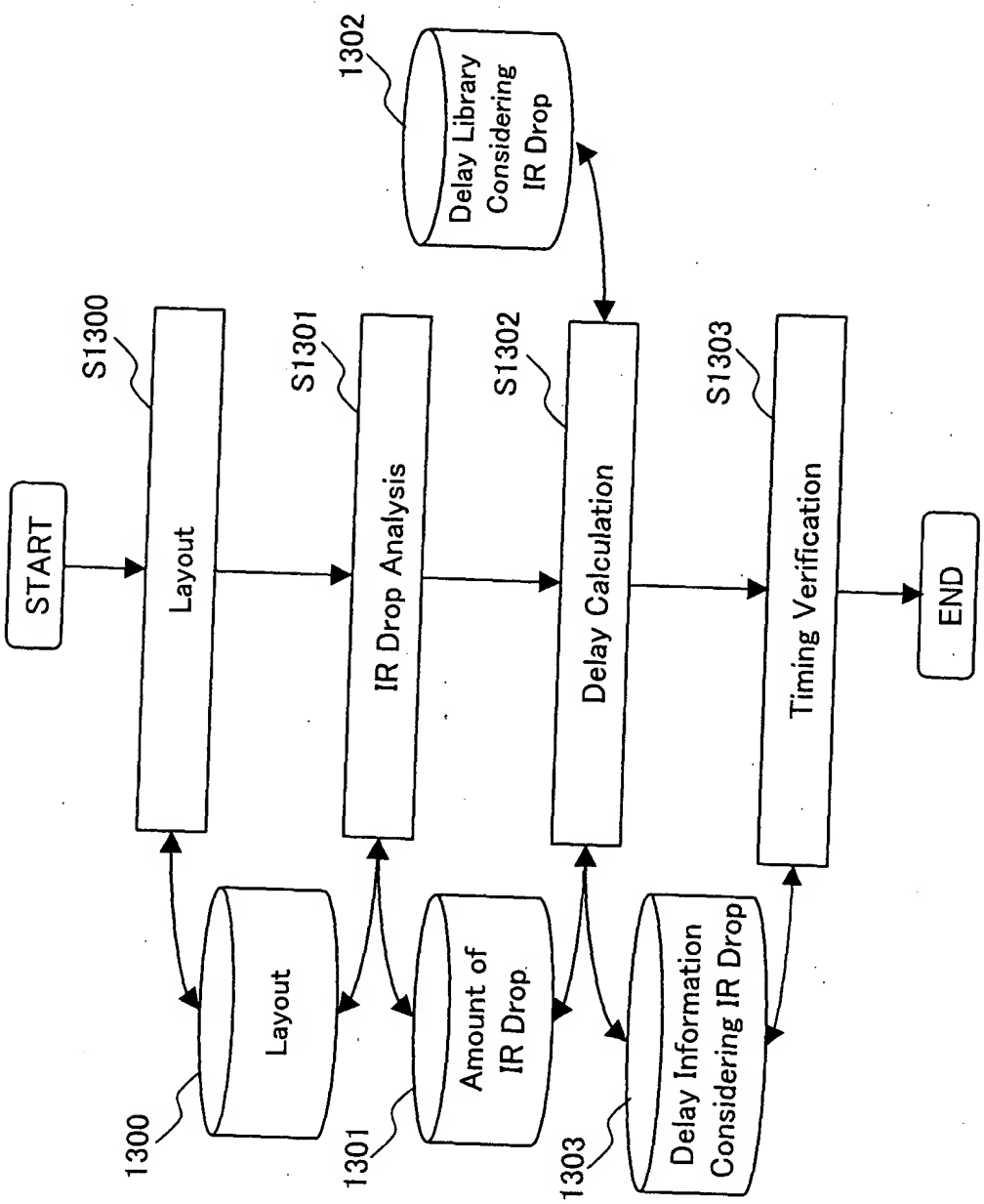

FIG. 13
PRIOR ART

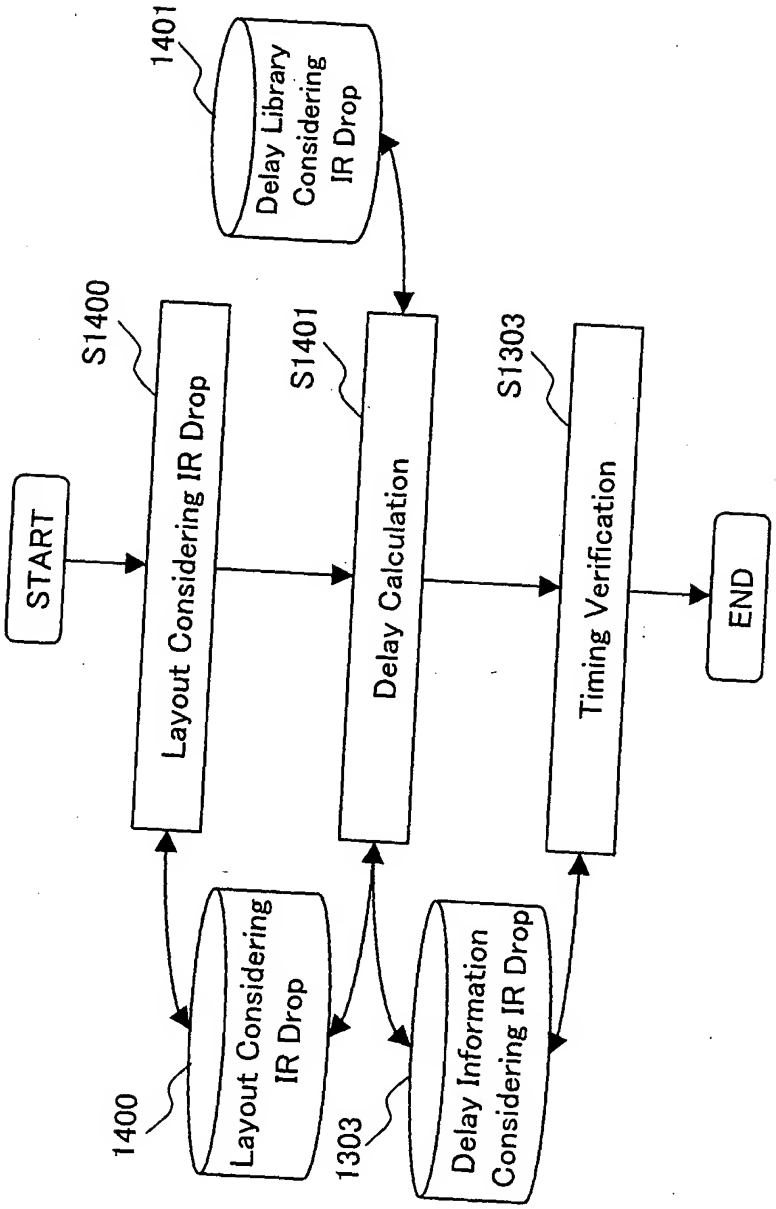

FIG. 14
PRIOR ART